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EXAMINER	
UMEZ ERONINI, LYNETTE T	
ART UNIT	**PAPER NUMBER**
1765	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/674,700	YE ET AL.	
	Examiner	Art Unit	
	Lynette T. Umez-Eronini	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,17,18 and 20-28* is/are rejected.

7)☒ Claim(s) *16 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9/29/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 6, 9, 10, 11, 12, 17, 18, 22-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Dai et al. (US 5,935,762).

Dai discloses, " . . . forming dual damascene patterns using a silylation process. A substrate is provided with a tri-layer of insulation formed thereon. A first layer of silylation photoresist is formed on the substrate and is imaged with a hole pattern by exposure through a mask. Using a silylation process, . . . , the regions in the first photoresist adjacent to the hole pattern are affixed to form top surface imaging mask. The hole pattern is then etched in the first photoresist. A second layer of photoresist is formed, and is imaged with a line pattern aligned with the previous hole pattern by exposure through a mask. The line pattern in the second photoresist is etched. The hole pattern in the first photoresist is transferred into the top layer of composite insulation first and then into the middle etch-stop layer by successive etching. The line pattern in the second photoresist layer is transferred into the first photoresist layer through a subsequent resist dry etching process. Finally, the line pattern and the hole pattern are transferred simultaneously into the top and lower layers of the composite

insulation layer, respectively, through a final dry oxide etching. Having thus formed the integral hole and line patterns into the insulation layer, metal is deposited into the dual damascene pattern. Any excess metal on the surface of the insulating layer is then removed by any number of ways including chemical-mechanical polishing, thereby planarizing the surface and readying it for the next semiconductor process" (Abstract). The aforementioned reads on,

A method of fabricating an interconnect structure, comprising:

(a) providing a substrate having a film stack formed thereon;

b) patterning and etching a first feature in the film stack;

(c) forming a bi-layer mask comprising an organic film and an imaging film on the film stack;

(d) patterning the bi-layer mask;

(e) etching a second feature in the film stack using the patterned bi-layer mask as an etch mask; and

(f) metallizing the first and second features to form the interconnect structure, **in claims 1, 22, 28; and 28**;

wherein the first barrier layer comprises at least one of silicon dioxide (SiO_2) and silicon nitride (Si_3N_4), **in claim 6**;

wherein the first feature is a trench and the second feature is a contact hole, **in claim 9**;

wherein the first feature is a contact hole and the second feature is a trench, **in claim 10**;

wherein the first feature is formed by patterning and etching a trench in the film stack to a pre-determined depth, **claim 11**;

wherein the second feature is formed by patterning a contact hole in the bi-layer mask, **in claim 12**;

wherein the first feature is formed by patterning and etching a contact hole in the film stack to a predetermined depth, **in claim 17**;

wherein the second feature is formed by patterning a trench in the bi-layer mask, **in claim 18**;

wherein the trench is etched to a predetermined depth in the film stack, **in claim 23**; and

wherein the contact hole is etched to a predetermined depth in the film stack, **in claim 26**.

Since Dai uses the same method of forming an interconnecting structure as claimed by applicants, then using Dai's method in the same manner as claimed by applicants would inherently result wherein the step (e) further comprises: using a portion of the organic film in the trench as an etch mask so as to remove lithographic misalignment between the contact hole and the trench when the contact hole is etched, in claims **24 and 27**.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 2-5, 7, 8, 14, 15, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dai (US 762) as applied to claims 1, 6, 9, 10, 11, 12, 17, and 18 above, and further in view of Chen et al. (US 6,809,028 B2).

Dai differs in failing to disclose the specific film stack and materials that comprise the capping, sacrificial, first dielectric, second dielectric, first barrier, second barrier, and metal layer as specified in the following:

wherein the film stack comprises a first barrier layer, a conductive layer embedded in a first dielectric layer, a second barrier layer and a second dielectric layer, **in claim 2**;

wherein at least one of a capping layer and a sacrificial layer is formed on the second dielectric layer, **in claim 3**;

wherein the sacrificial layer comprises at least one of amorphous silicon, titanium nitride (TiN) and tungsten (W), **in claim 4**.

wherein the first dielectric layer and the second dielectric layer each comprise at least one of carbon doped silicon oxide, organic doped silicon glass and fluorine doped silicon glass, **in claim 5**;

wherein the second barrier layer comprises silicon carbide (SiC), **in claim 7**; and.

wherein the conductive layer comprises at least one of copper (Cu), aluminum (Al), tantalum (Ta), tungsten (W), titanium (Ti), tantalum nitride (TaN) and titanium nitride (TiN), **in claim 8.**

Chen teaches fabricating dual damascene copper by providing a semiconductor substrate **20** with a first insulating layer **21** (same as applicants' first barrier layer) over the substrate **20**,; followed by a patterning copper interconnection wiring **23** in an embedded second insulating layer **22** (same as applicants' first insulating layer), which overlies insulating layer **21**; then depositing an etch stop layer **24** (same as applicants' second barrier layer) over insulating layer **22** and copper wiring **23**; and forming a third insulating layer **25** (same as applicants' second insulating layer) over layer **24** (column 4, lines 2-32 and **FIGS. 2A-2E**). Chen also teaches using dielectric insulators such as fluorinated silicate glass and Xerogels (column 2, lines 41-51) and etch-stop layers (same as applicants' barrier layer) such as SiN and SiC (column 3, lines 4, lines 18-20).

Since Chen illustrates interconnecting structures comprising stacked layers and materials comprising the capping, sacrificial, first dielectric, second dielectric, first barrier, second barrier, and metal layer are known, then it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to employ such materials to accomplish the claimed invention for the purpose of improving the method of making semiconductor devices (Chen, column 1, lines 8-10).

Dai also differs in failing to teach wherein step (b) comprises: etching the trench in the film stack comprising a dielectric material to a pre-determined depth by providing carbon tetrafluoride (CF_4) and nitrogen (N_2) at a CF_4:N_2 flow ratio in a range from 1:4 to 2:3, **in claim 14**;

wherein step (e) comprises: etching the contact hole in the organic layer to a pre-determined depth by providing ammonia (NH_3) and oxygen (O_2) at a flow ratio NH_3:O_2 in a range from 1:1 to 100 percent ammonia, **in claim 15**;

etching the hole in the film stack comprising a dielectric material to a pre-determined depth by providing carbon tetrafluoride (CF_4) and nitrogen (N_2) at a CF_4:N_2 flow ratio in a range from 1:4 to 2:3, **in claim 20**; and

wherein step (e) comprises: etching the trench in the organic layer to a pre-determined depth by providing ammonia (NH_3) and oxygen (O_2) at a flow ratio NH_3:O_2 in a range from 1:1 to 100 percent ammonia, **in claim 21**.

Chen teaches the insulating layer is reactive ion etched by a process chemistry selected from the group of gases comprised of CF_4 and is combined with ambient gas mixtures selected from the group comprised of O_2 and N_2 (column 4, lines 39-45).

Since Chen illustrates the specific combination of CF_4 and N_2 and also NH_3 and O_2 etchants is known, then it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to select any flow ratio of CF_4 and N_2 as well as select any percent ratio of NH_3:O_2 in the Chen reference that would effectively accomplish the disclosed composition because it has been held that there is no invention where the difference in proportions is not critical and was ascertained by routine experimentation because the determination of workable ranges is not considered inventive. See In re Swain and Adams, 70 USPQ 412 (CPA 1946).

6. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dai (US '569) as applied to claim 1 above, and further in view of Hopper (US 6,576,545 B1).

Dai differs in failing to teach a step comprising a step of planarizing the metallized interconnect structure to remove the sacrificial layer and at least a portion of the capping layer.

Hopper teaches removing a barrier layer (same as applicants' sacrificial layer) in a trench/via structure that is filled with a conductive metal is removed by chemical mechanical polishing to form a device with dual damascene interconnect (column 9, line 11-17).

Since Hopper illustrates planarizing a metal layer along with a barrier layer is known, then it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to use a known method of planarizing a conductive structure as taught by Hopper for the purpose of removing excess conductive material in completing the damascene structure (Hopper, column 9, lines 14-17).

Allowable Subject Matter

7. Claim 13 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: Applicants' Remarks were persuasive in showing the Chen reference fails to teach or suggest using a portion of the organic film in the trench as an etch mask so as to remove lithographic misalignment between the contact hole and the trench when the contact hole is etched, as recited in claims 13 and 19.

Response to Arguments

9. Applicant's arguments filed 12/30/2005 have been fully considered but they are not persuasive. Applicants traversed the rejection of claims 1, 6, 9-12, and 22-28 under 35 U.S.C. 102(b) as being anticipated by Dai (US 5,935,762). Applicants argued Dai teaches a process wherein the first time any feature is etched into the film stack (the hole pattern) occurs after both the first photoresist and the second photoresist are

formed and patterned. Therefore, Dai fails to teach or suggest patterning and etching a first feature (trench in claim 22) in the film stack and then forming a bi-layer mask comprising an organic film and an imaging film on the film stack; patterning the bilayer mask; and etching a second feature (contact hole in claim 22) in the film stack using the patterned bi-layer mask as an etch mask, as recited in independent claims 1 and 22.

Applicants' arguments are unpersuasive because Dai teaches a method of fabricating an interconnect structure (Abstract), as claimed by applicants. The claims do not require a method of forming a trench before forming a contact hole.

10. Applicants traversed the rejection of claims 2-5, 7-8, 13-15, and 19-21 under 35 U.S.C. 103(a) as being obvious in light of Dai (US '762) in view of Chen et al. (US 6,809,028).

Applicant's arguments, see Remarks, filed 12/30/2005, with respect to claims 13 and 19 have been fully considered and are persuasive. The rejection of claims 13 and have been withdrawn.

11. Applicants traversed the rejection of claim 16 under 35 U.S.C. 103(a) as being obvious in light of Dai (US '762) in view of Hopper et al. (US 6,576,545) and argued Hopper may not be used to modify Dai in a manner that would yield the limitations recited in claim 1.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention

where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, since Hopper illustrates planarizing a metal layer along with a barrier layer is known, then it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to use a known method of planarizing a conductive structure as taught by Hopper for the purpose of removing excess conductive material in completing the damascene structure (Hopper, column 9, lines 14-17).

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynette T. Umez-Eronini whose telephone number is 571-272-1470. The examiner is normally unavailable on the First Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Art Unit 1765

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March 2, 2006

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER